TRANSISTOR AND MEMORY CELL WITH ULTRA-SHORT GATE FEATURE AND METHOD OF FABRICATING THE SAME

ABSTRACT OF THE DISCLOSURE

In one embodiment of the present invention, a method of forming semiconductor transistors includes: forming a gate electrode over but insulated from a semiconductor body region; forming off-set spacers along side-walls of the gate electrode; and after forming said off-set spacers, forming a source region and a drain region in the body region so that the extent of an overlap between the gate electrode and each of the source and drain regions is dependent on a thickness of the off-set spacers. In another embodiment, a method of forming a non-volatile memory cell includes: forming a first polysilicon layer over but insulated from a semiconductor body region; forming a second polysilicon layer over but insulated from the first polysilicon layer; forming an off-set spacer along at least one side-wall of the first and second polysilicon layers; and after forming said off-set spacer, forming at least one of source and drain regions in the body region so that the extent of an overlap between the first polysilicon layer and said one of source and drain regions is dependent on a thickness of the off-set spacer.